IN THE CLAIMS

1. (Original) An apparatus, comprising:

a content addressable memory (CAM) array;

an output register coupled to the CAM array, the output register configured to output data based on a delayed clock signal; and

a programmable delay circuit coupled to receive a reference clock signal and generate the delayed clock signal using a delay element.

2. (Original) The apparatus of claim 1, wherein the programmable delay circuit comprises:

a plurality of the delay elements to generate a plurality of delayed clock signals;

a programmable register to store information indicating a particular delayed clock signal of the plurality of delayed clock signals; and

a multiplexer coupled with the programmable register and the plurality of delay elements to select the particular delayed clock signal based on the information.

3. (Original) The apparatus of claim 2, wherein the programmable delay circuit further comprises a decoder coupled to the programmable register to decode the information stored in the programmable register.

4. (Original) The apparatus of claim 2, wherein each of the plurality of delay elements provides a different time period of delay to the reference clock signal.

5. (Original) The apparatus of claim 4, wherein one of the plurality of delay elements provides substantially a zero time period of delay.

6. (Original) The apparatus of claim 4, wherein at least one of the plurality of delay elements comprises a series of inverters.

7. (Original) The apparatus of claim 1, wherein the reference clock signal is received at a clock pad and wherein the programmable delay circuit is coupled between the clock pad and the output register.

8. (Original) The apparatus of claim 7, further comprising a second programmable delay circuit coupled between the first programmable delay circuit and the output register.

9. (Original) The apparatus of claim 8, wherein the programmable delay circuit and the second programmable delay circuit each comprise a separate programmable register.

10. (Original) The apparatus of claim 7, further comprising an instruction decoder coupled to the clock pad to receive the reference clock signal.

11. (Original) The apparatus of claim 2, wherein the information for the programmable register indicates the particular delayed clock signal according to a frequency of the reference clock signal.

12. (Original) The apparatus of claim 1, wherein the programmable delay circuit is a first programmable delay circuit comprising:

a first plurality of the delay elements to generate a first plurality of delayed clock signals;

a first programmable register to store first information indicating a first particular delayed clock signal of the first plurality of delayed clock signals; and

a first multiplexer coupled with the first programmable register and the first plurality of delay elements to select the first particular delayed clock signal based on the first information, and wherein the apparatus further comprises a second programmable delay circuit coupled with the first programmable delay circuit.

13. (Original) The apparatus of claim 12, wherein the second programmable delay circuit comprises:

a second plurality of the delay elements to receive the first particular delayed clock signal and generate a second plurality of delayed clock signals;

a second programmable register to stored second information indicating a second particular delayed clock signal of the second plurality of delayed clock signals; and

a second multiplexer coupled with the second programmable register and the second plurality of delay elements to select the second particular delayed clock signal based on the second information.

14. (Original) The apparatus of claim 12, wherein the second programmable delay circuit comprises:

a second plurality of the delay elements to receive the first particular delayed clock signal and generate a second plurality of delayed clock signals, the first programmable register for storing second information indicating a second particular delayed clock signal of the second plurality of delayed clock signals; and

a second multiplexer coupled with the first programmable register and the second plurality of delay elements to select the second particular delayed clock signal based on the second information.

15. (Original) The apparatus of claim 7, further comprising a processor coupled to the clock pad to transmit the reference clock signal.

16. (Original) The apparatus of claim 1, further comprising a processor coupled with the output register to receive the data.

17. (Original) The apparatus of claim 1, further comprising a read circuit coupled between the CAM array and the output register.

18. (Original) The apparatus of claim 1, wherein the CAM array comprises a plurality of rows of CAM cells each having a corresponding match line.

19. (Original) The apparatus of claim 18, further comprising a match flag circuit coupled to the match lines and the output register.

20. (Original) The apparatus of claim 18, further comprising an encoder circuit coupled to the match lines and the output register.

21. (Original) An apparatus, comprising:

a content addressable memory (CAM) array;

a clock circuit coupled to the CAM array; and

a programmable delay circuit coupled to receive a reference clock signal and generate a programmable delayed clock signal using a delay element for the clock circuit.

22. (Original) The apparatus of claim 21, wherein the programmable delay circuit comprises:

a plurality of the delay elements to generate a plurality of delayed clock signals;

a programmable register to store information indicating a particular delayed clock signal of the plurality of delayed clock signals; and

a multiplexer coupled with the programmable register and the plurality of delay elements to select the particular delayed clock signal based on the information.

23. (Original) The apparatus of claim 22, wherein the programmable delay circuit further comprises a decoder coupled to the programmable register to decode the information stored in the programmable register.

24. (Original) The apparatus of claim 22, wherein each of the plurality of delay elements provides a different time period of delay to the reference clock signal.

25. (Original) The apparatus of claim 21, wherein the clocked circuit comprises a read circuit for reading data from the CAM array.

26. (Original) The apparatus of claim 21, wherein the clocked circuit comprises a register for storing comparand data for comparison with data of the CAM array.

27. (Original) The apparatus of claim 21, wherein the CAM array comprises a plurality of rows of CAM cells each having a corresponding match line for carrying a match signal indicative of whether comparand data matches data of the corresponding row of CAM cells.

28. (Original) The apparatus of claim 27, wherein the clocked circuit comprises an encoder circuit coupled to the match lines and the programmable delay circuit.

29. (Original) The apparatus of claim 28, wherein the clocked circuit comprises match flag logic coupled to the match lines and the programmable delay circuit.

30. (Original) The apparatus of claim 21, further comprising:

a second clocked circuit; and

a second programmable delay circuit.

Claims 31-42 (Canceled)

43. (Original) A method, comprising:

establishing a connection with a register in a content addressable memory (CAM) device; and

programming the register in the content addressable memory (CAM) device with information representing a value of a delay time period for the generation of a delayed clock signal.

44. (Original) The method of claim 43, further comprising:

generating the delayed clock signal based on a reference clock signal using the programmed information; and

outputting data based on the delayed clock signal.

45. (Original) The method of claim 44, further comprising:

programming the register with additional information representing the value of another delay time period; and

generating the delayed clock signal using the additional information.

46. (Original) The method of claim 44, further comprising:

programming a second register with second information representing the value of a second delay time period; and

generating the delayed clock signal using the second information.

47. (Original) The method of claim 46, further comprising programming the second programmed information based on an anticipated frequency of operation for the reference clock signal.

Claims 48-50 (Canceled)

51. (Original) An apparatus configured to operate based on a reference clock signal, comprising:

a content addressable memory (CAM) array;

means for generating a delayed clock signal using at least one delay element in response to the reference clock; and

a clocked circuit coupled to receive the delayed clock signal.

52. (Original) The integrated circuit device of claim 51, wherein the means for generating comprises means for generating the delayed clock signal using first and second programmed information representing values of first and second delay time periods, respectively.

53. (Original) The integrated circuit device of claim 52, further comprising means for programming the second programmed information based on an anticipated frequency of operation for the reference clock signal.